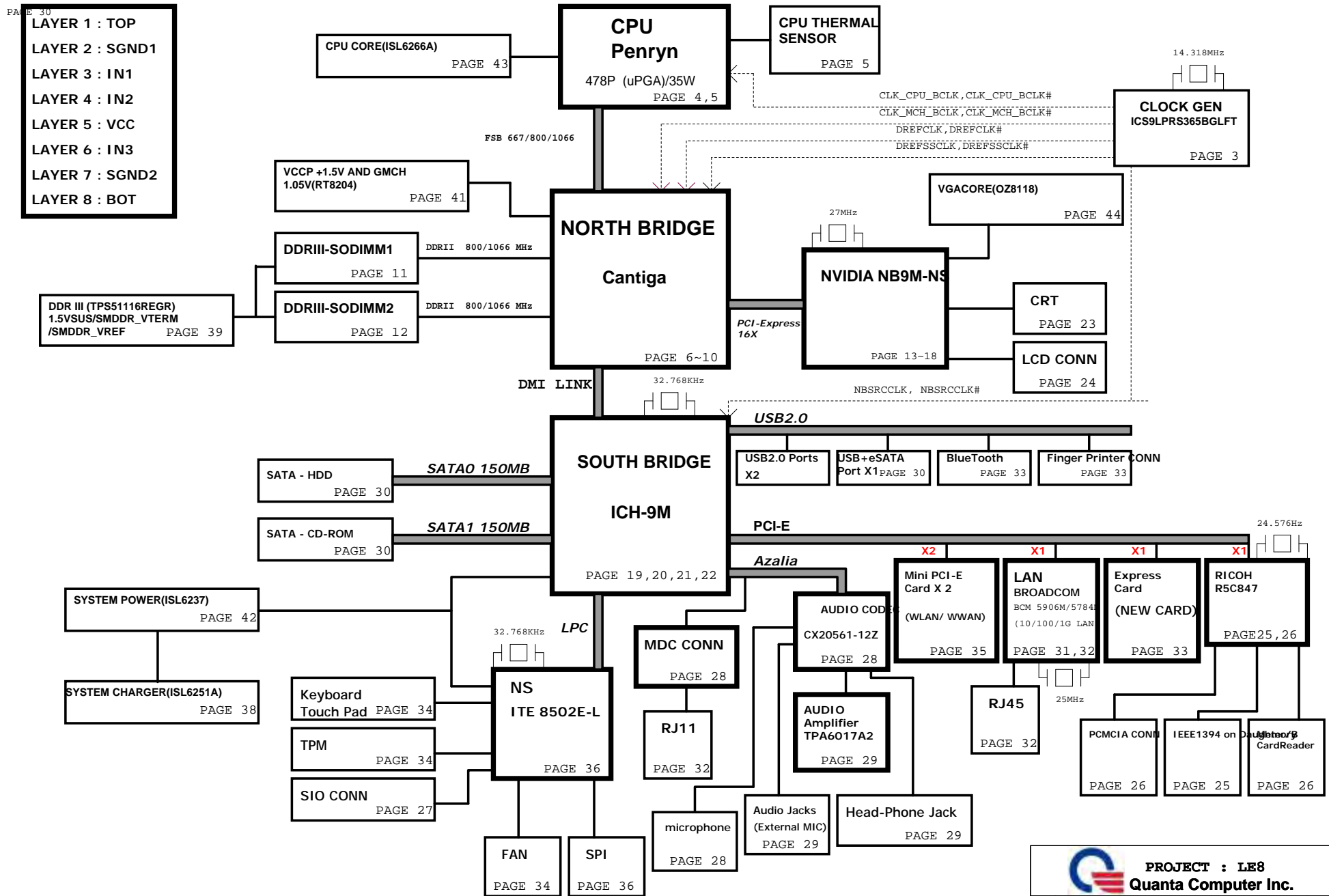


PCB STACK UP
8L

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

LE9E(LE8) BLOCK DIAGRAM

01

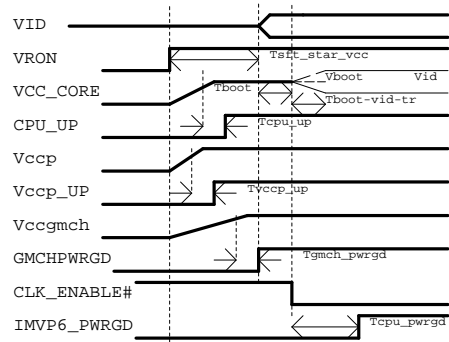


Board Stack up Description

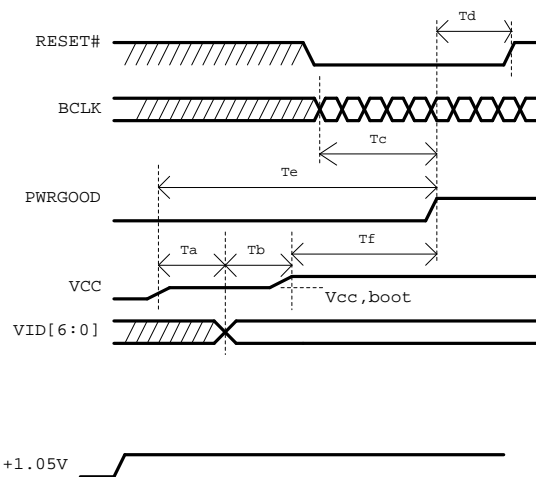
PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



MEROM Power-up Timing Specifications

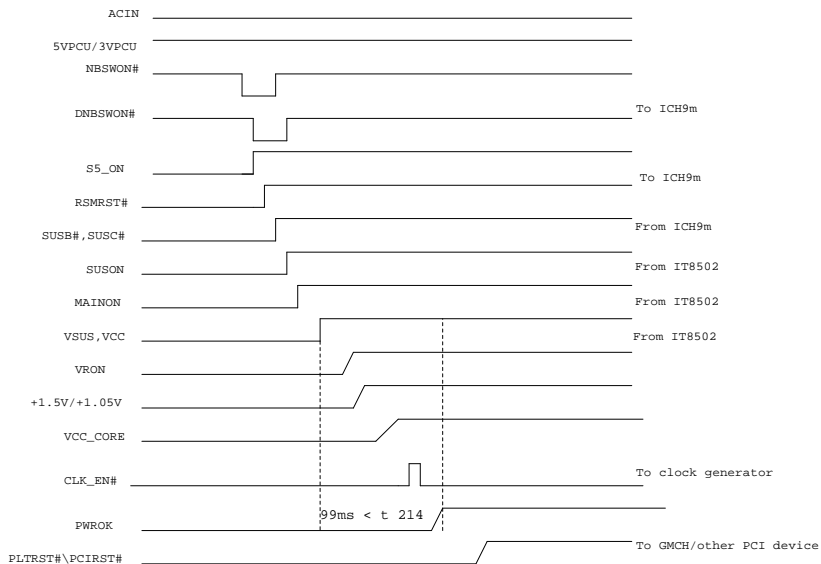


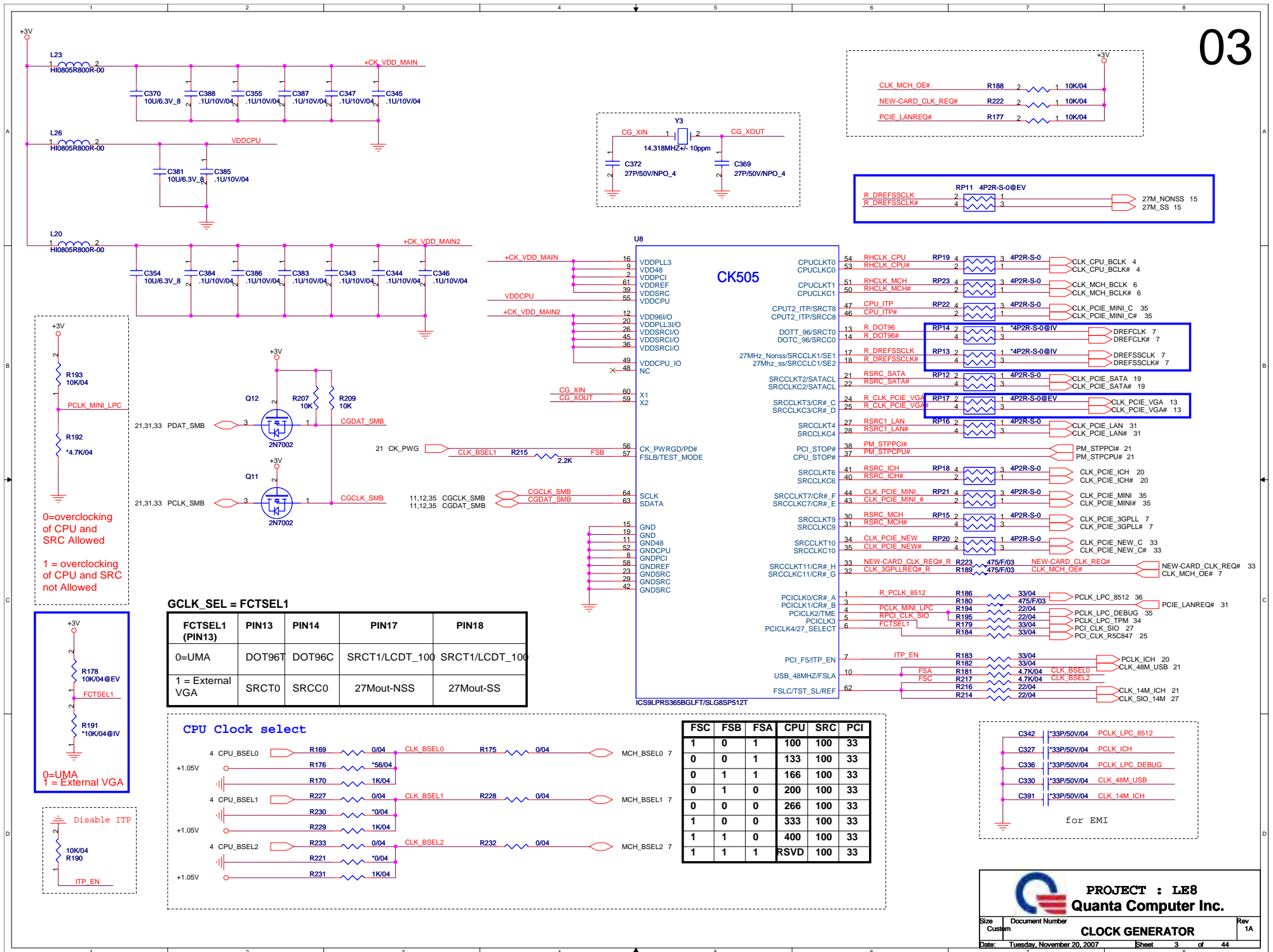
Ta=VCC and VCCP assertion to VID[6:0] valid
 Tb=VID[6:0] stable to VCC valid
 Tc=BCLK stable to PWRGOOD assertion
 Td=PWRGOOD to RESET# de-assertion time
 Te=Vcc,boot valid to PWRGOOD assertion time

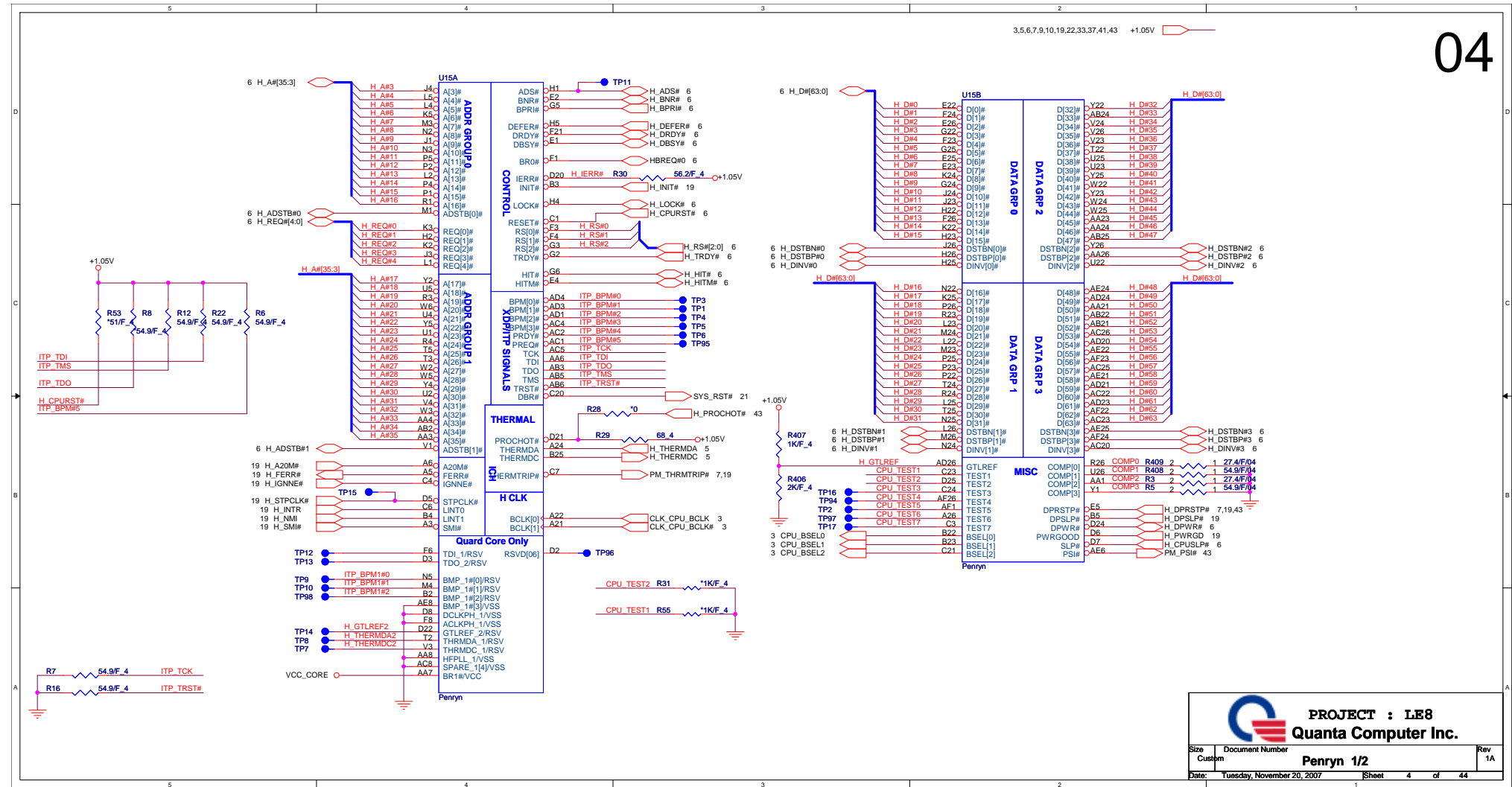
Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.5VSUS	X	X			SUSON
SMDRR_VTERM/+3V/+5V/+15V/+1.8V	X				MAINON
+VGACORE/+VGA1.1V	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

ACIN POWER ON TIMING

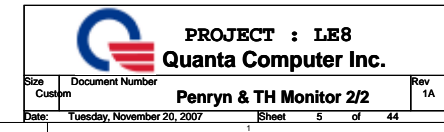






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Quanta Computer Inc.

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Sheet 4 of 44
Rev 1A



3.5,10,11,12,13,15,16,19,20,21,22,23,24,25,26,27,28,30,31,33,34,36,37,38,40,41,42,43,44
+3V
8.10,11,12,33,37,39,44 1.5VSUS
3.4,5,6,9,10,19,22,33,37,41,43 1.05V_PEG
10 +1.05V_PEG

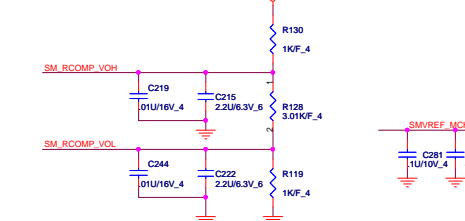
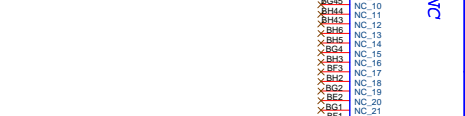
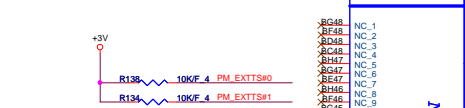
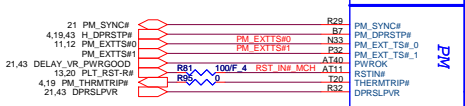
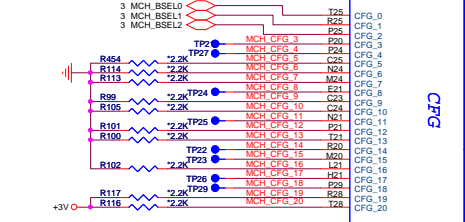
07

- MCH_CFG_5 DMIX2 selection
Low: DMIX2
High: DMIX4 (Default)
MCH_CFG_16 FSB Dynamic ODT
Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)
MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)
MCH_CFG_19 DMI Lane Reversal
Low: Normal (Default)
High: Lane Reserved
MCH_CFG_6 ITPM Host Interface
Low: ITPM Host Interface enabled
High: ITPM Host Interface disabled (Default)
MCH_CFG_7 Intel (R) Management Engine Crypto
Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

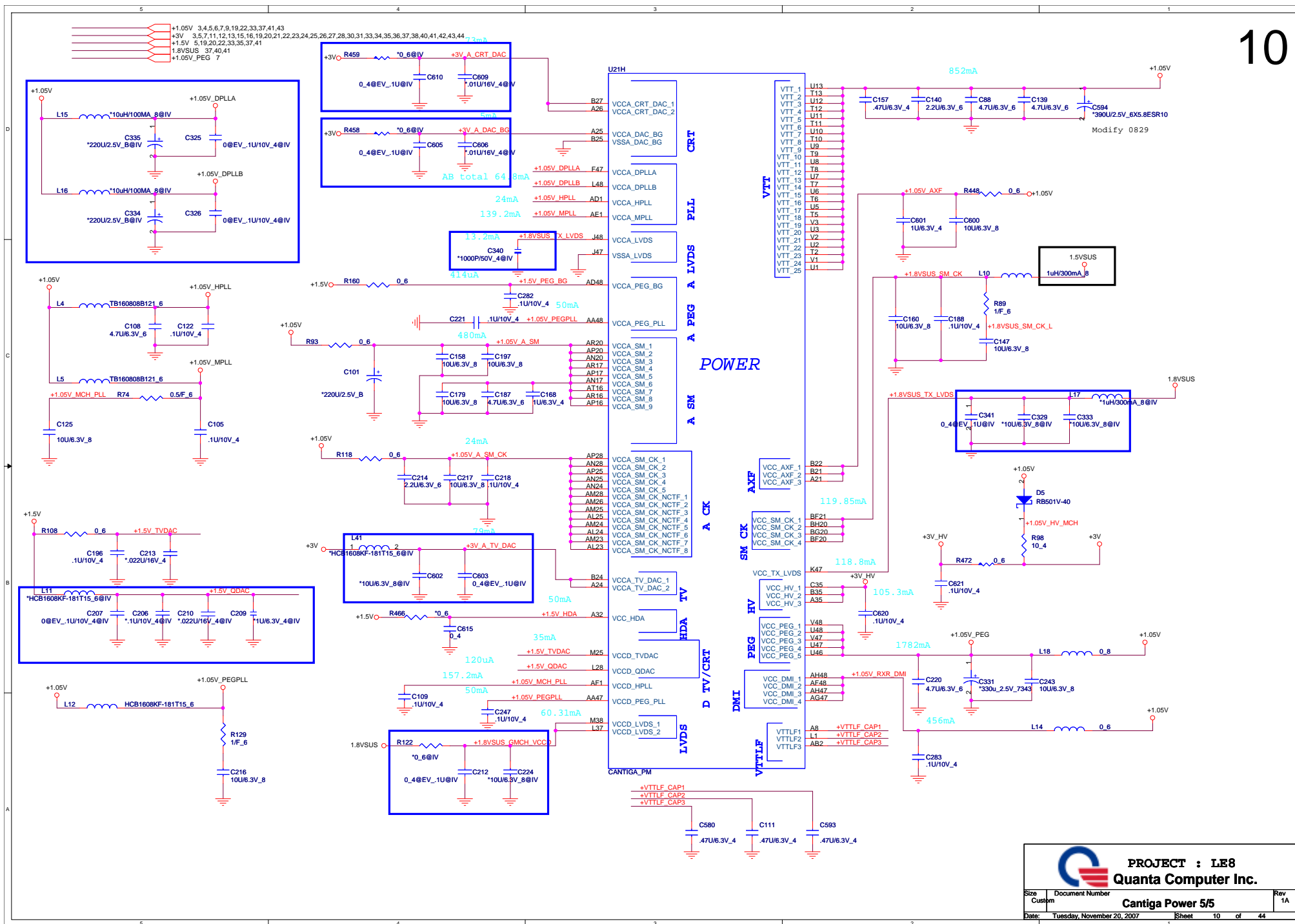
- MCH_CFG_10 PCIe Lookback Enable
Low: Enabled
High: Disabled (Default)
MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating
MCH_CFG_13 MCH_CFG_12 Configuration

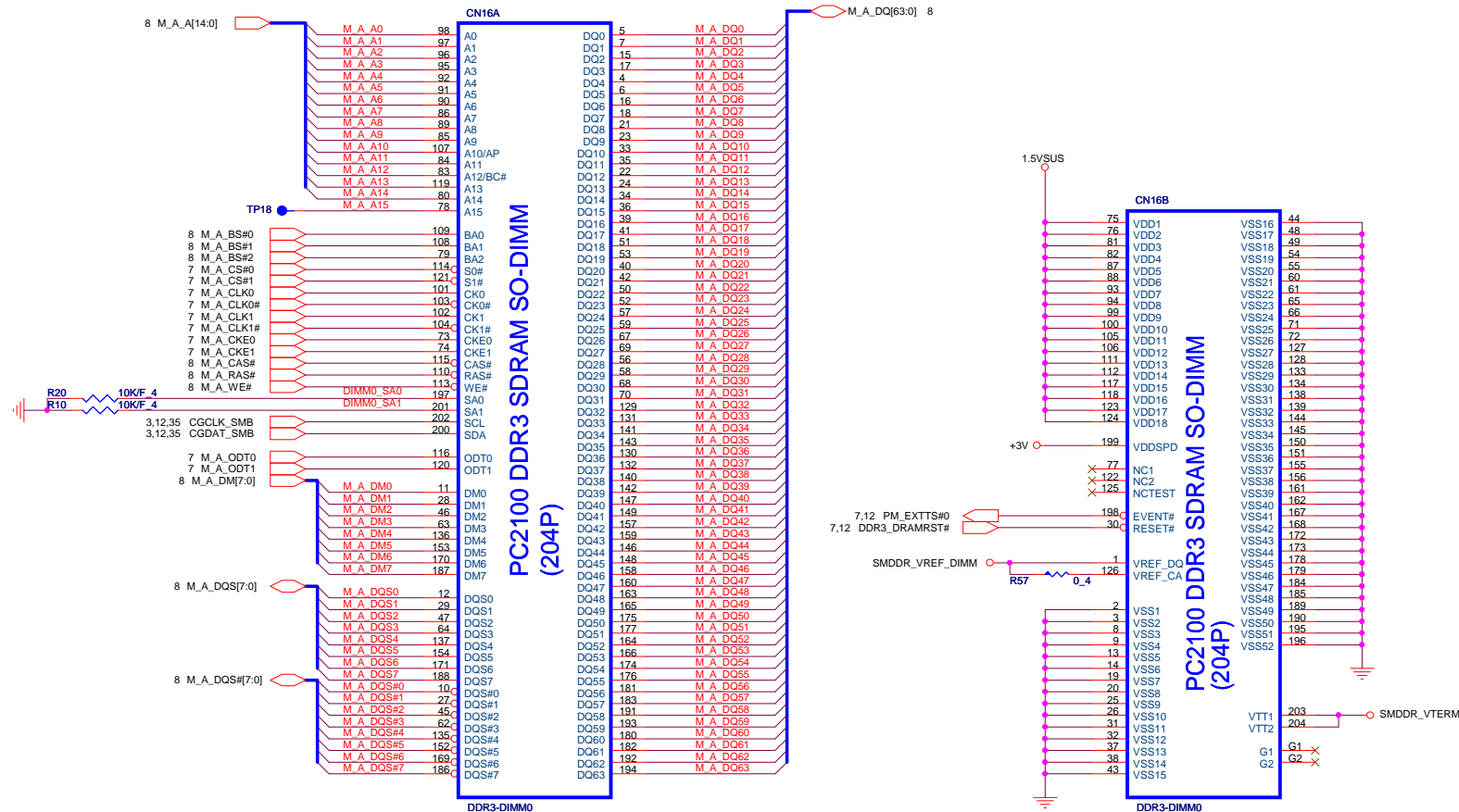
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

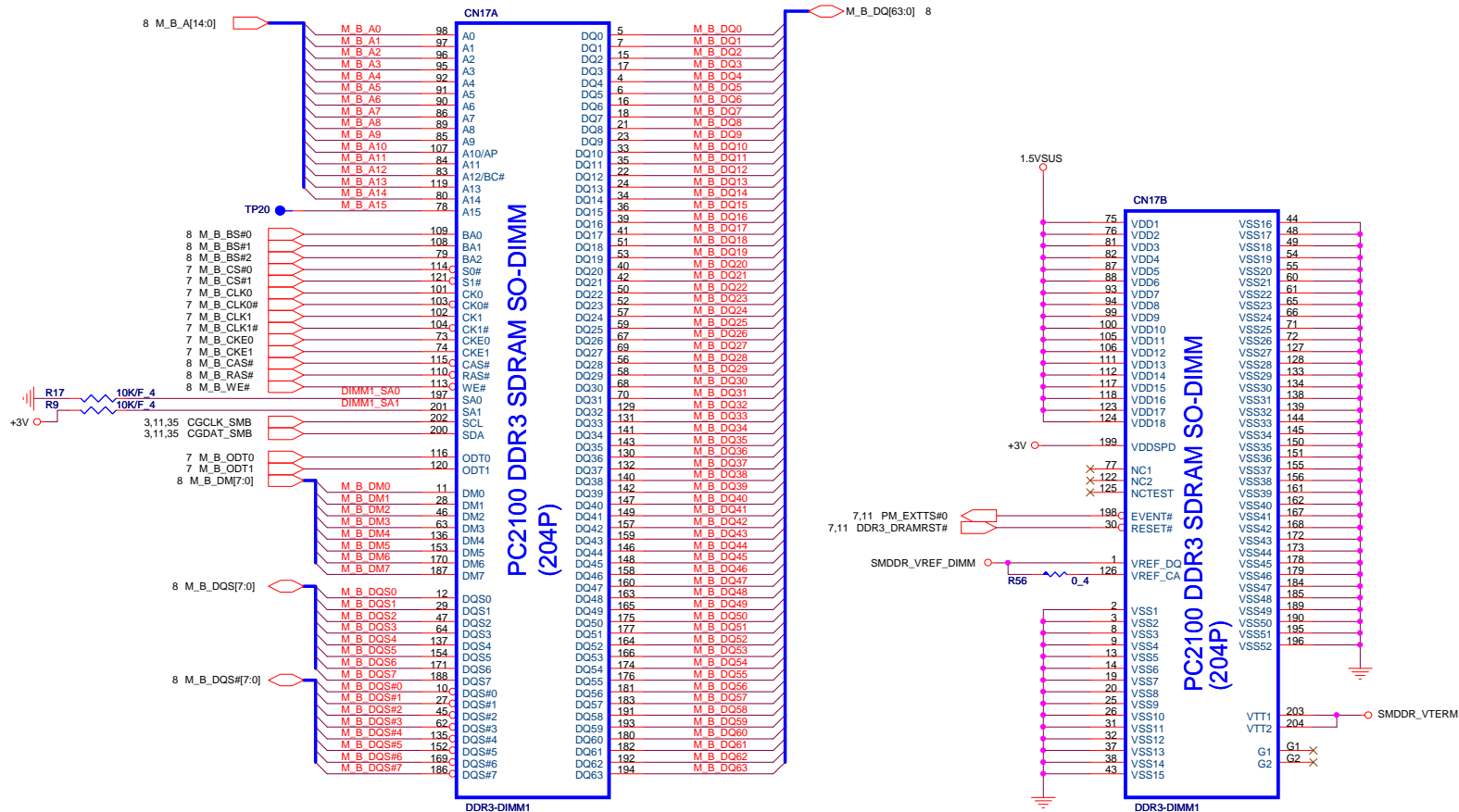
- TP30 AL34 ME_JTAG_TCK
TP30 AN35 ME_JTAG_TDO
TP30 AM35 ME_JTAG_TMS

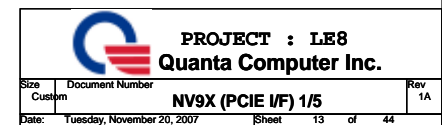


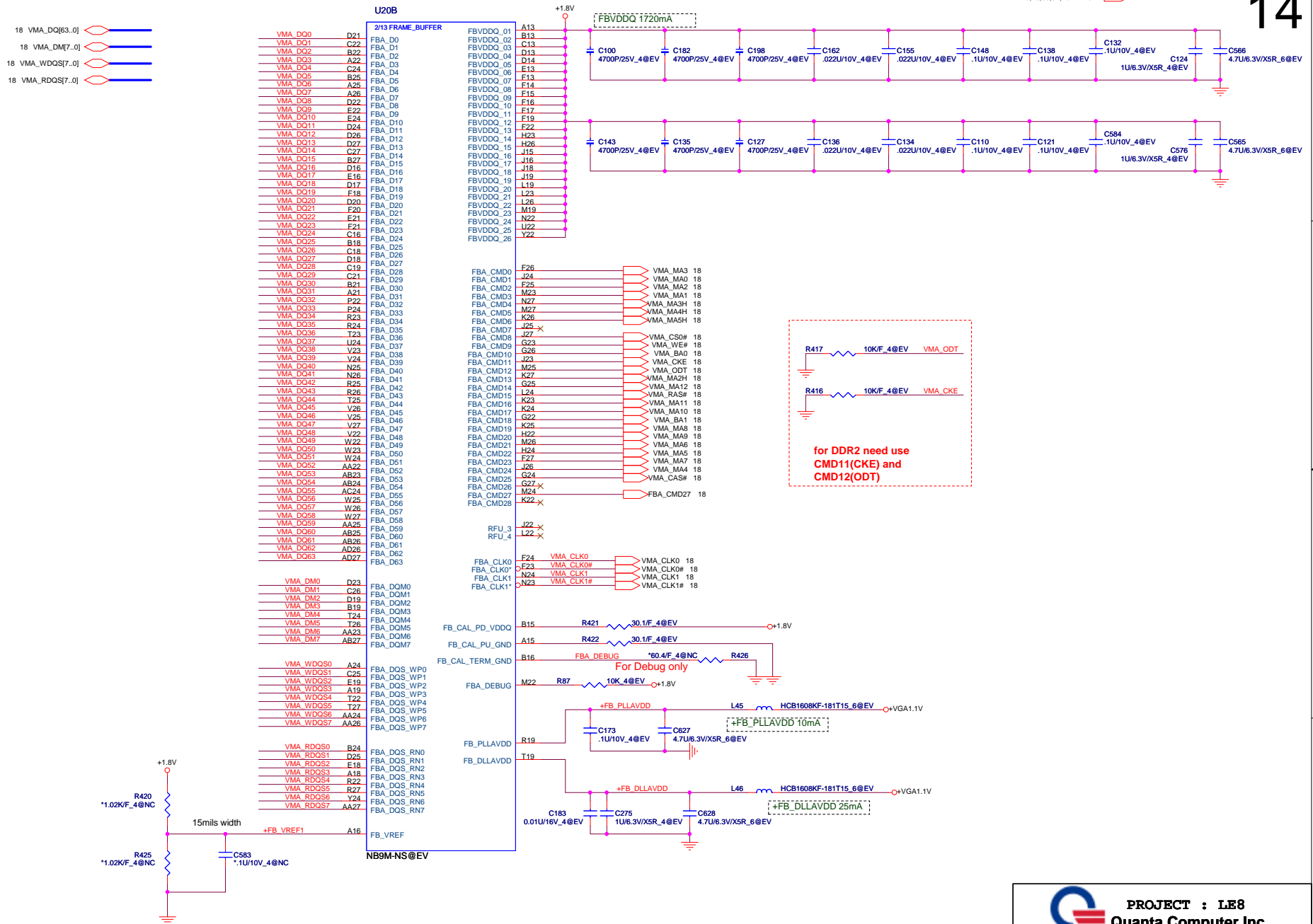


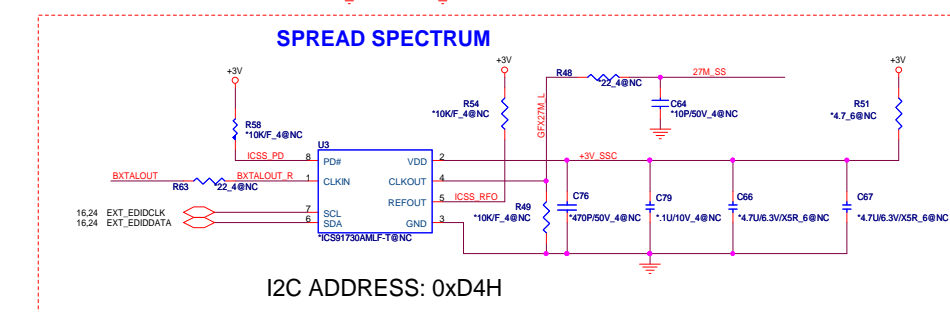
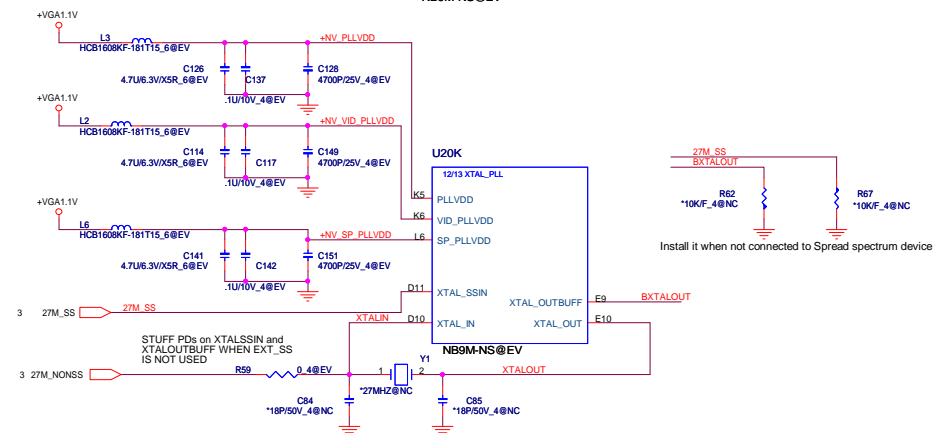
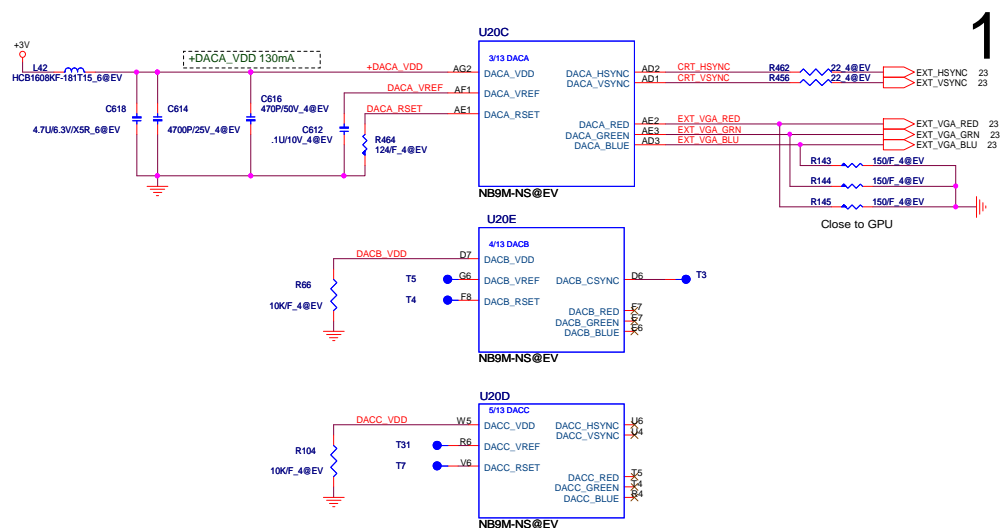




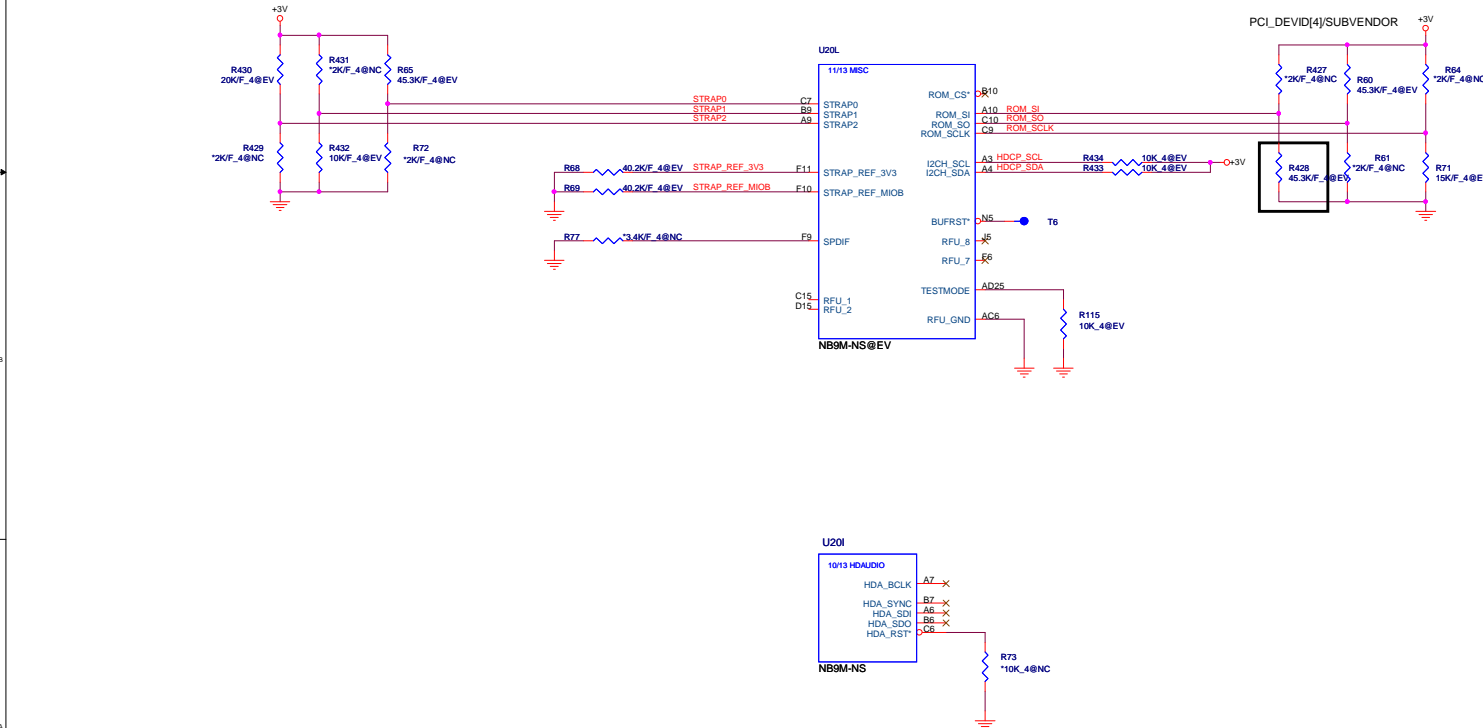









GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	NVGEM HOTPLUG DETECT
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD ALTVO
6	OUT	HIGH	NVVDD ALTV1
7	OUT	HIGH	FBVDD VID0
8	IN	LOW	OVERTEMP ALERT
9	OUT	LOW	THERMAL ALERT
10	OUT	HIGH	DYNAMIC FB VREF GDDR3(not used for DDR2)
11	OUT	HIGH	SLI SYNC0(not used for GB1-64)
12	IN	N/A	AC DETECT
13	OUT	LOW	POWER SUPPLY CONTROL0
14	OUT	HIGH	POWER SUPPLY CONTROL1
15	IN	N/A	HPD_E
16	IN	N/A	DVI_E
17	IN	N/A	HDMI_E
18	IN	N/A	DVI_F(not used)
19	IN	N/A	HDMI_F(not used)



NB9M-NS VRAM Configuration Table	
ROM_SI	VRAM CONFIG SET

STRAP	VALUE		MEMORY Vendor
0	5K	PD	NOT USED
1	10K	PD	Samsung DDR2 16Mx16
2	15K	PD	Qmnd DDR2 16Mx16
3	20K	PD	HYNX DDR2 16Mx16
4	25K	PD	NOT USED
5	30K	PD	Samsung DDR2 32Mx16
6	35K	PD	Qmnd DDR2 32Mx16
7	45K	PD	HYNX DDR2 32Mx16

		PROJECT : LE8 Quanta Computer Inc.	
Size C	Document Number NV9X (GPIO & STRRAPS) 4/5	Rev 1A	
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U20J

13/13 GND_NC

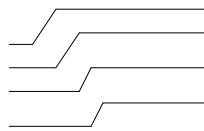
AC11	GND_01	NC_01	AA6
AC14	GND_02	NC_02	AC19
AC17	GND_03	NC_03	E15
AC2	GND_04	NC_04	T6
AC20	GND_05		
AC23	GND_06		
AC26	GND_07		
AC5	GND_08		
AC8	GND_09		
AE11	GND_10		
AE14	GND_11		
AE17	GND_12		
AE2	GND_13		
AE20	GND_14		
AE23	GND_15		
AE26	GND_16		
AE5	GND_17		
AE8	GND_18		
B11	GND_19		
B14	GND_20		
B17	GND_21		
B2	GND_22		
B20	GND_23		
B23	GND_24		
B26	GND_25		
B5	GND_26		
B8	GND_27		
E11	GND_28		
E14	GND_29		
E17	GND_30		
E2	GND_31		
E20	GND_32		
E23	GND_33		
E26	GND_34		
E5	GND_35		
E8	GND_36		
H2	GND_37		
H5	GND_38		
J11	GND_39		
J14	GND_40		
J17	GND_41		
K19	GND_42		
K9	GND_43		
L11	GND_44		
L12	GND_45		
L13	GND_46		
L14	GND_47		
L15	GND_48		
L16	GND_49		
L17	GND_50		
L2	GND_51		
L5	GND_52		
M12	GND_53		
M13	GND_54		
M14	GND_55		
M15	GND_56		
M16	GND_57		
P19	GND_58		
P2	GND_59		
P23	GND_60		
P26	GND_61		
P5	GND_62		
P9	GND_63		
T12	GND_64		
T13	GND_65		
T14	GND_66		
T15	GND_67		
T16	GND_68		
U11	GND_69		
U12	GND_70		
U13	GND_71		
U14	GND_72		
U15	GND_73		
U16	GND_74		
U17	GND_75		
U2	GND_76		
U23	GND_77		
U26	GND_78		
U5	GND_79		
V19	GND_80		
V9	GND_81		
W11	GND_82		
W14	GND_83		
W17	GND_84		
Y2	GND_85		
Y23	GND_86		
Y26	GND_87		
Y5	GND_88		


NB9M-NS@EV

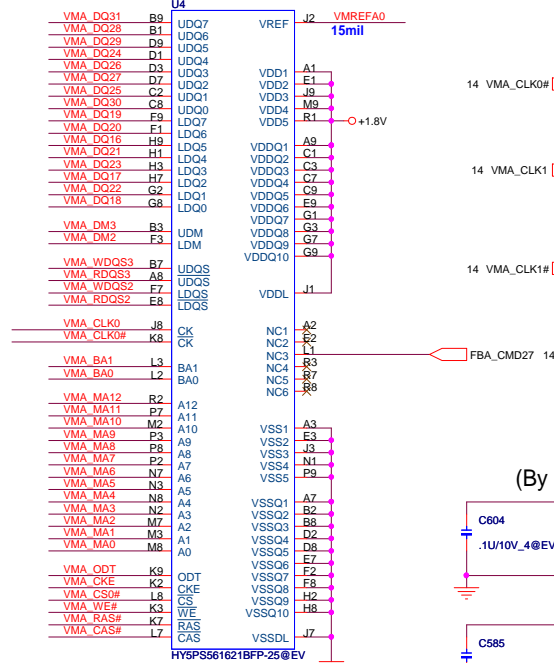
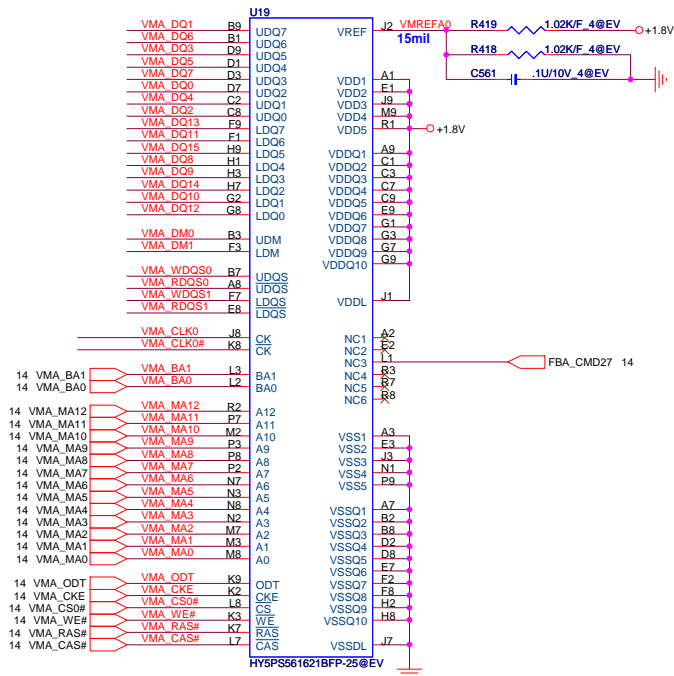
NB9M: VGACORE +0.9V ~ +1.0V

power up sequence

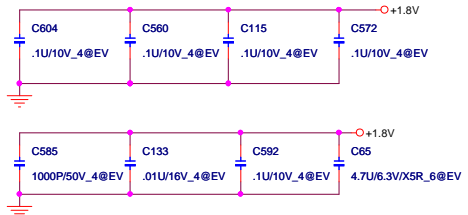
PXE 1.1VDD
I/O 3.3V
NVCORE
1.8VFBDDQ



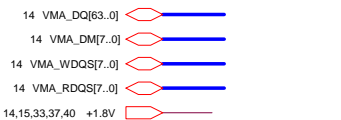
 PROJECT : LE8 Quanta Computer Inc.		Rev 1A
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(By pass capacitor)

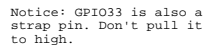


512Mb(32Mx16) : AKD5FG-TW31/Hynix(HY5PS121621CFP-25)
AKD5FG-T'04/Quimonda(HYB18T512161B2F-20)



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Quanta Computer Inc.

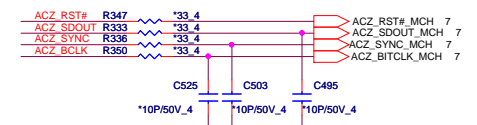
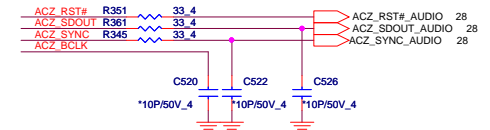
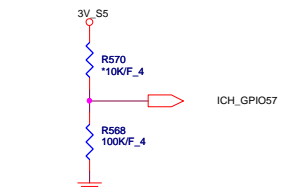
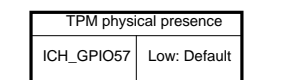
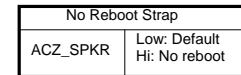
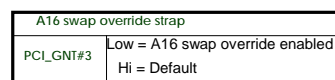
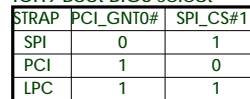
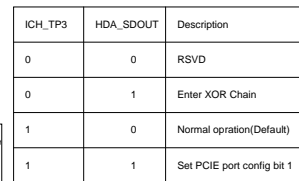
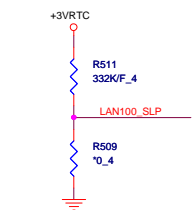
Size	Document Number	Rev
Custom	NV9X VRAM-1(GDDR2 BGA84)	1A
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ICH9-M Internal VR
Enable strap
(Internal VR for
Vccsus1_05,VccSus1_
and VccCL1_5)

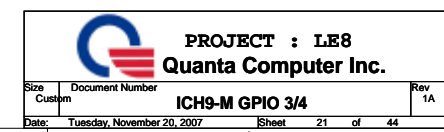
ICH9-M LAN100_SLP Strap
(Internal VR for
VccLAN1_05 and
VccCL1.05)

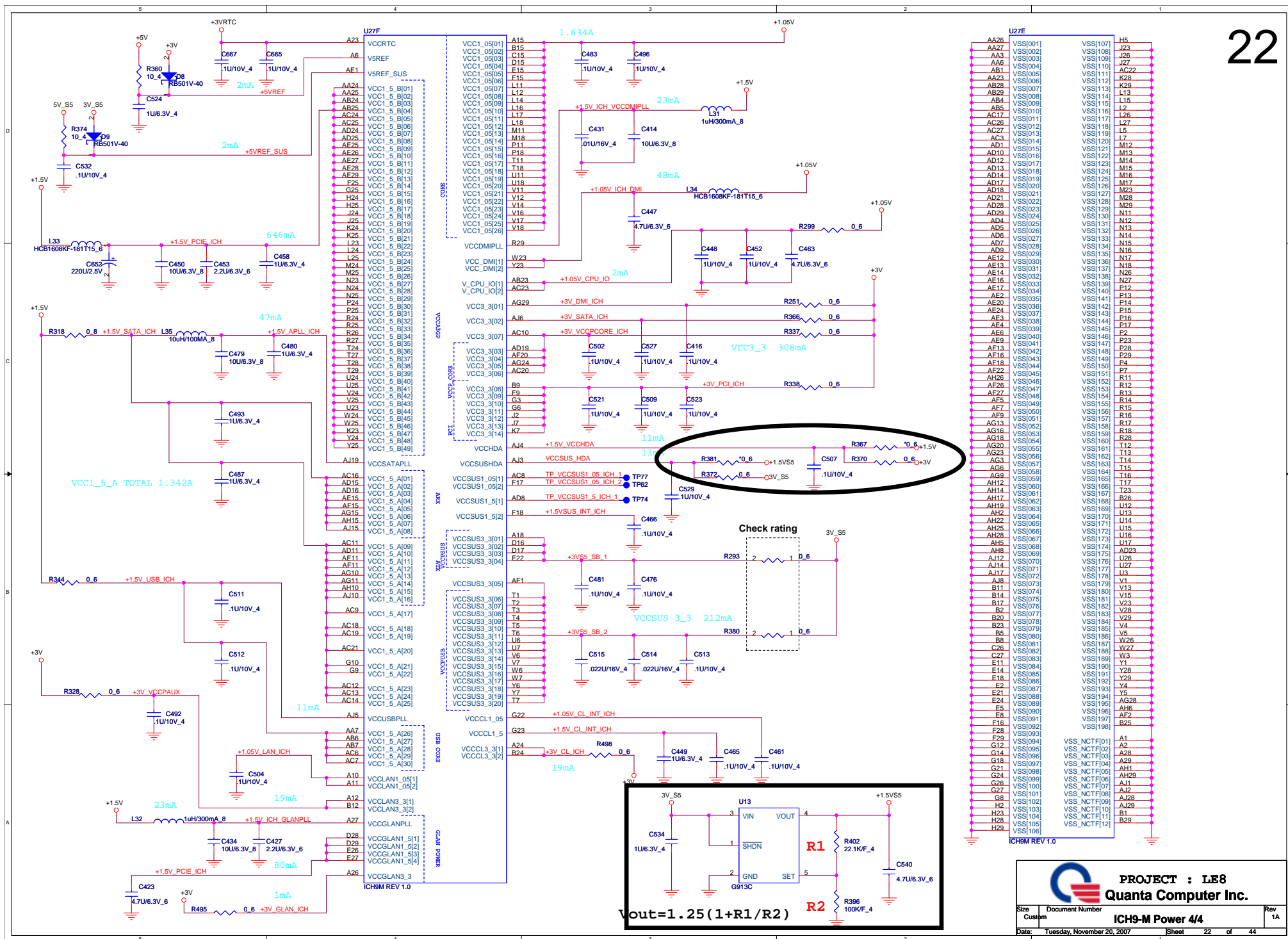
LAN100_SLP	Low = Internal VR disabled High = Internal VR enable(Default)
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		PROJECT : IE8 Quanta Computer Inc.	
Size Custom	Document Number ICH9-M Host 1/4	Rev 1A	
Date:	Tuesday, November 20, 2007	Sheet	19 of 44





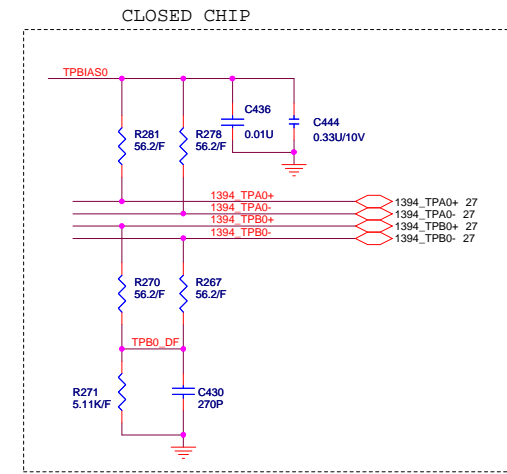





UMA & Discrete setting
LVDS Discrete / UMA

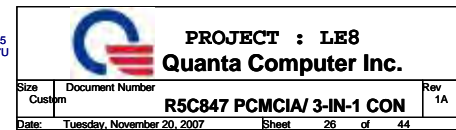
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R149	0	NC
R148	0	NC
R463	0	NC
R457	0	NC
R451	0	NC
R91	0	NC
R155	NC	0
R154	NC	0
R153	NC	0
R461	NC	0
R460	NC	0
R452	NC	0
R92	NC	0

Size Custom	Document Number CRT CON	Rev 1A
Date: Tuesday, November 20, 2007	Sheet 23 of 44	

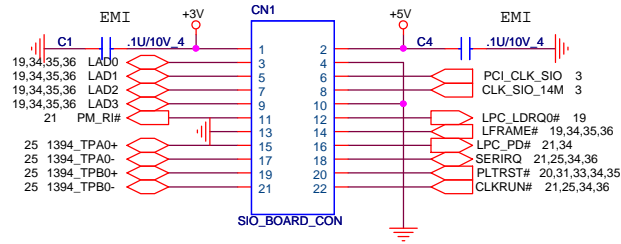


 <div style="text-align: right;"> PROJECT : LE8 Quanta Computer Inc. </div>		
Size Custom	Document Number <div style="text-align: center; font-size: 1.2em; font-weight: bold;">R5C847 PCI/1394</div>	Rev 1A
Date:	Tuesday, November 20, 2007	Sheet 25 of 44

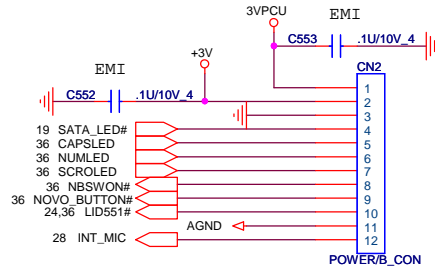
CN9
PCM CIA CON



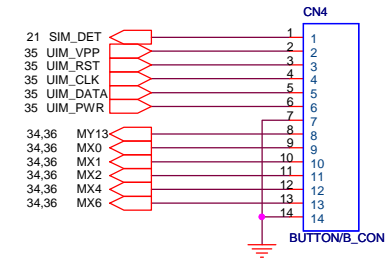
SIO BOARD



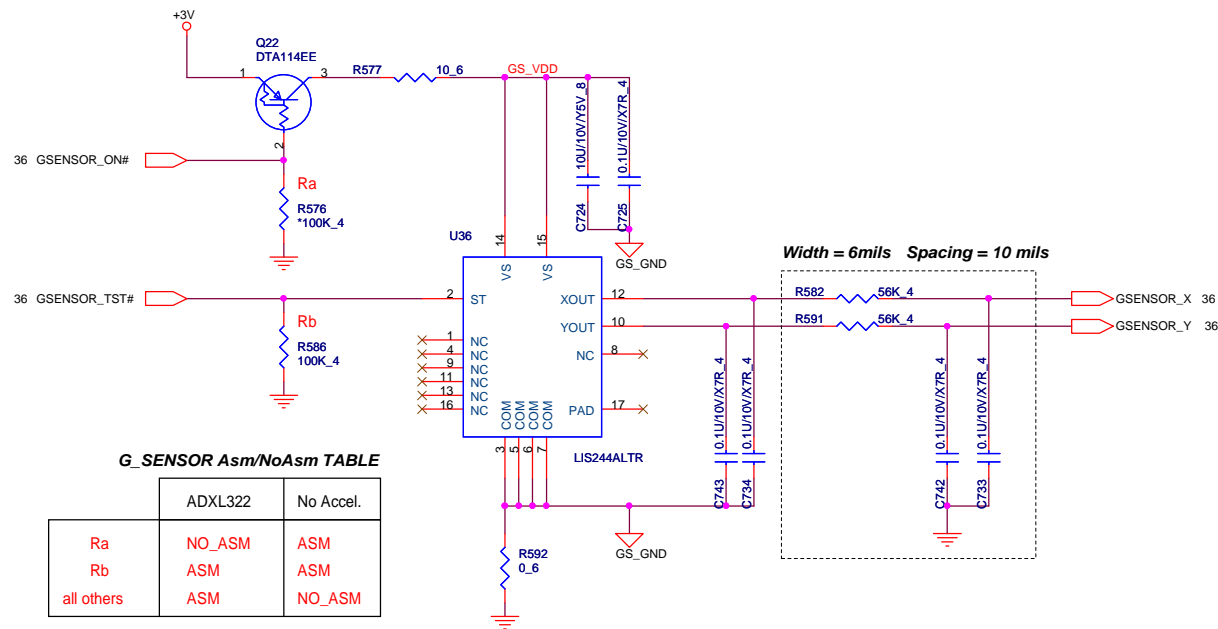
POWER BOARD



BUTTON BOARD

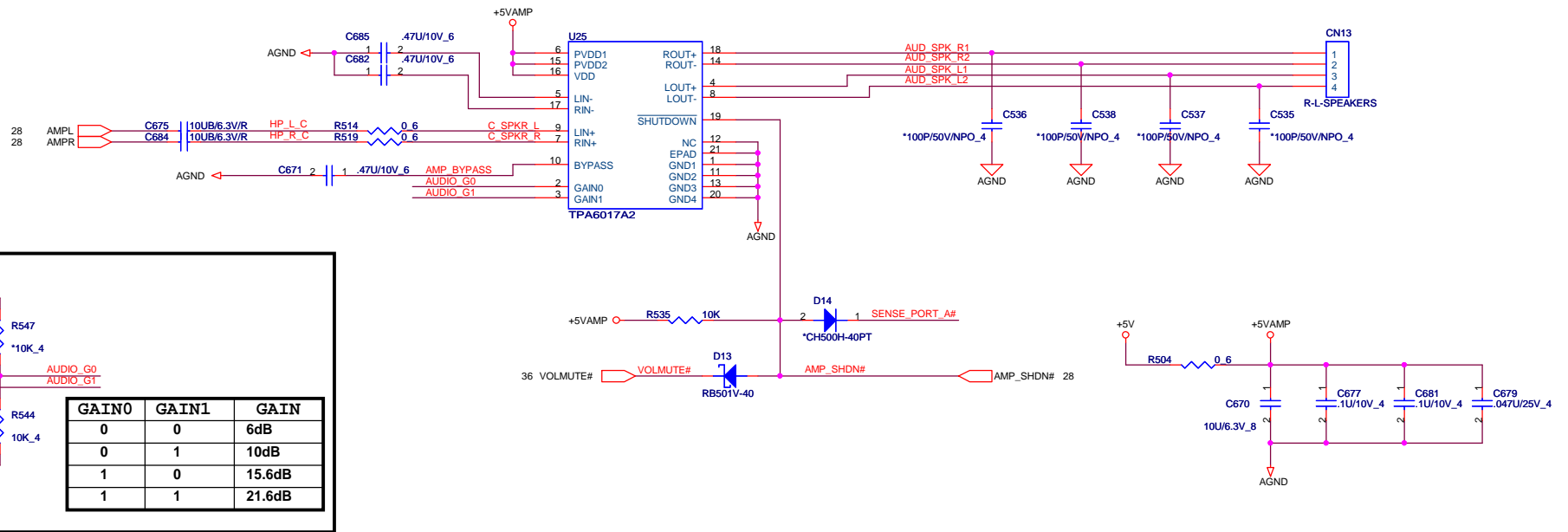


G-SENSOR

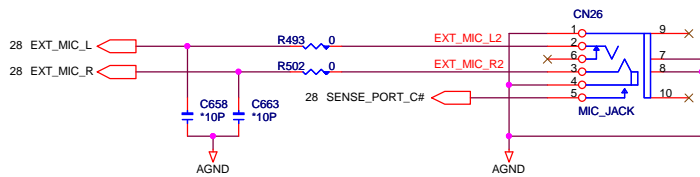


INTERNAL SPEAKER AMPLIFIER

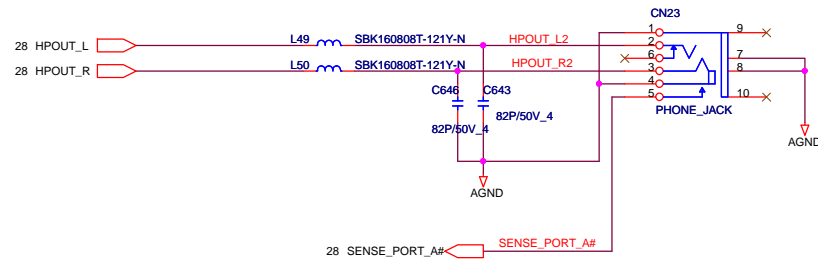
29




MIC-IN JACK



HEADPHONE

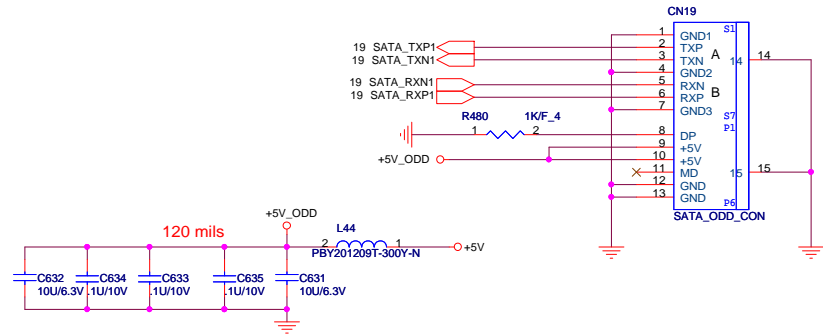




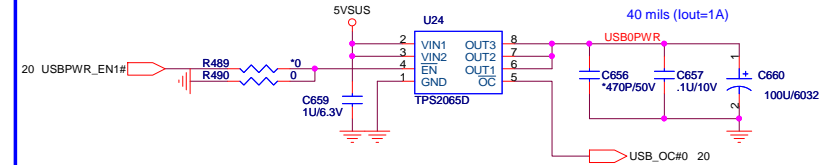
PROJECT : LE8
Quanta Computer Inc.

Size Custom	Document Number AMP_TPA6017 & JACKS	Rev 1A
Date: Tuesday, November 20, 2007	Sheet 29 of 44	

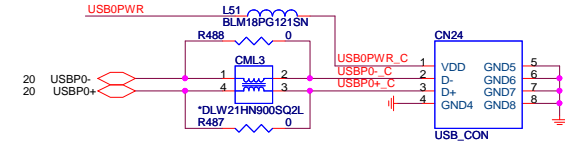
SATA CD-ROM



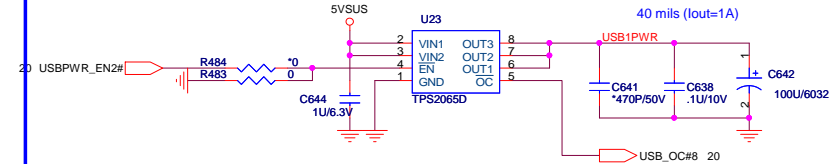
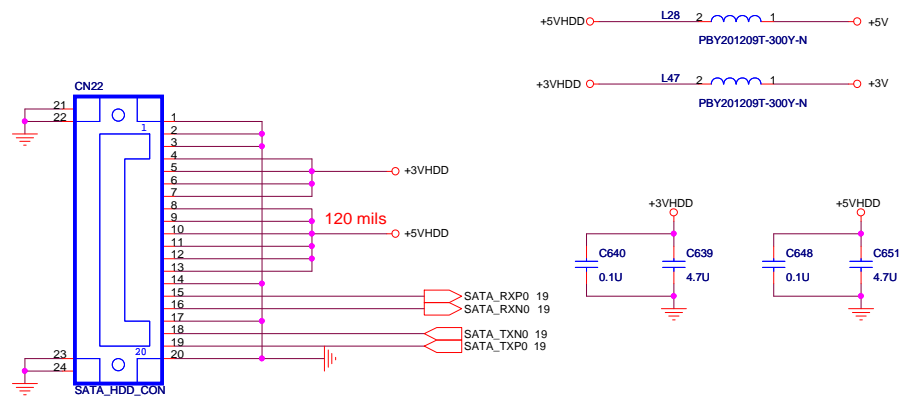
USBX2



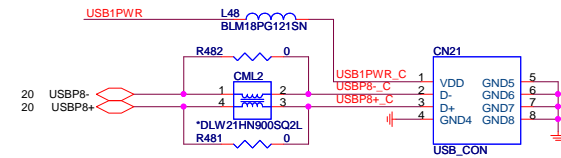
USB 0



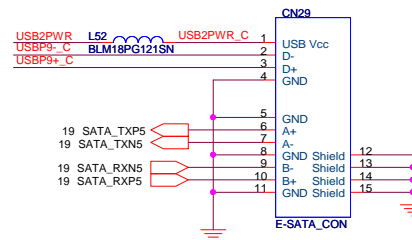
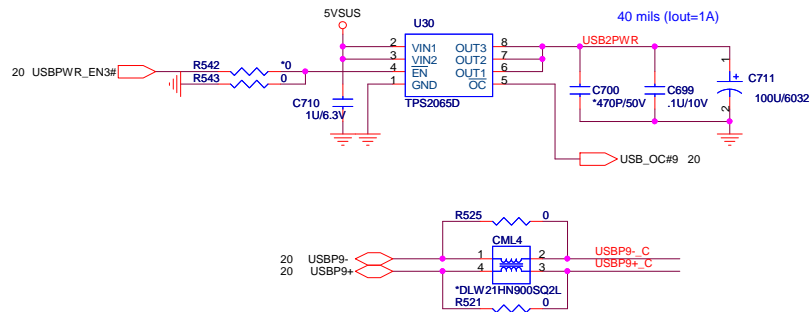
SATA-HDD CONNECTOR



USB 1



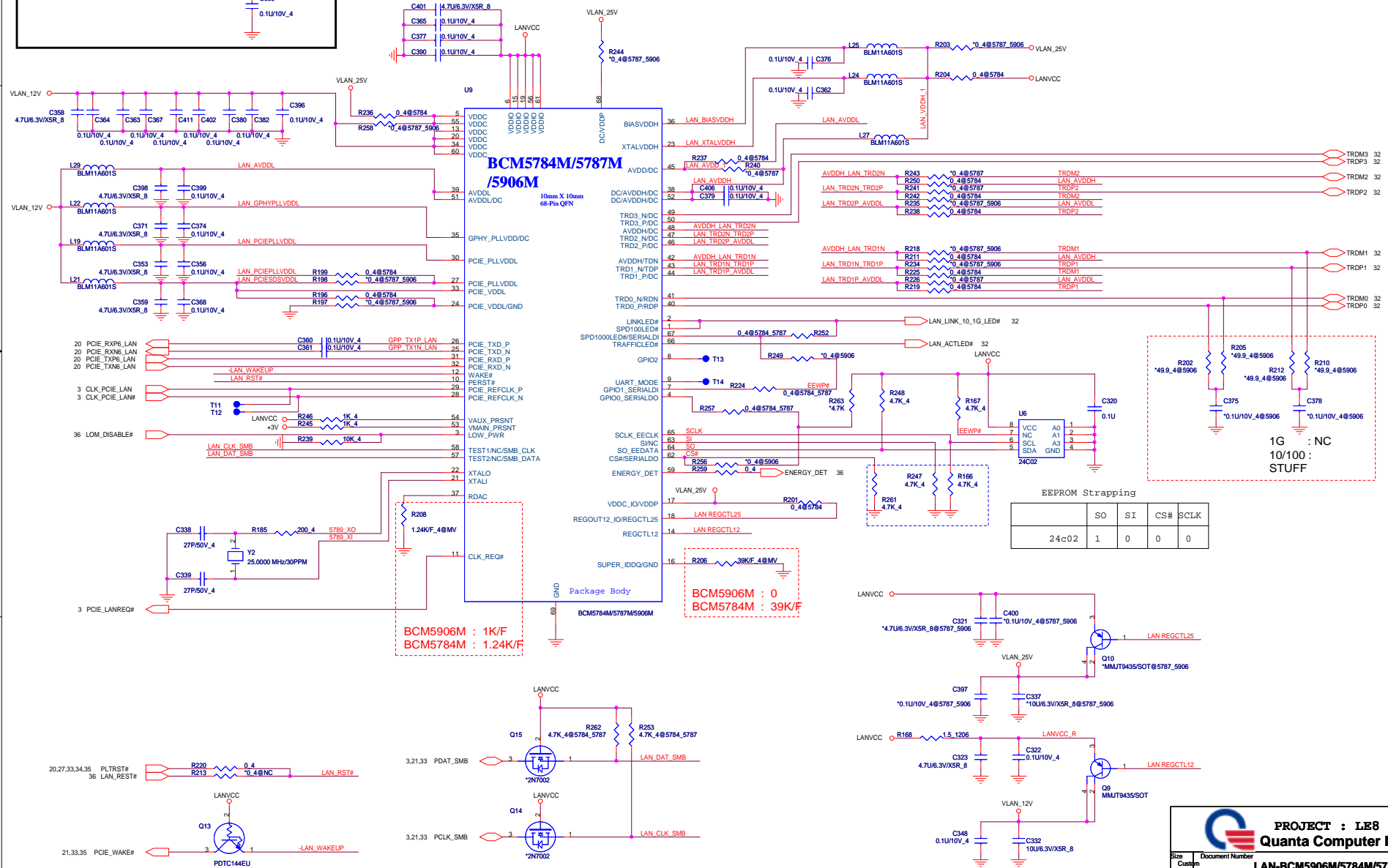
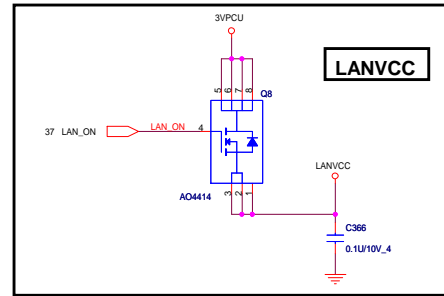
USB + eSATA CONNECTOR



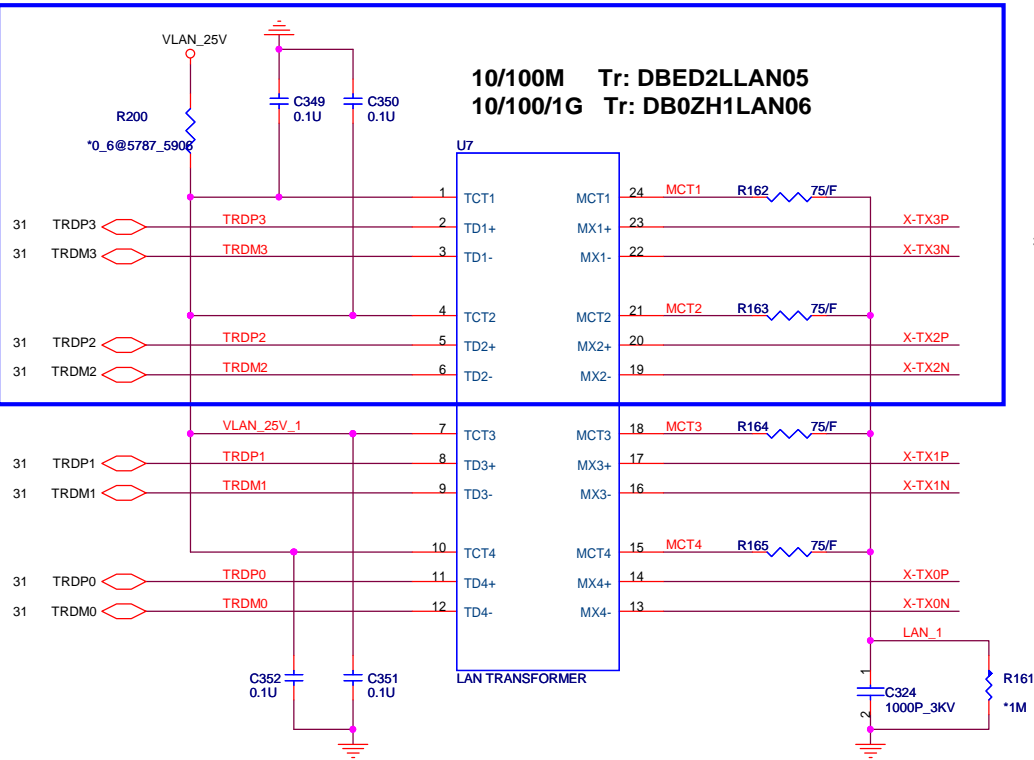
PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USB/ESATA	1A
Date:	Tuesday, November 20, 2007	Sheet 30 of 44

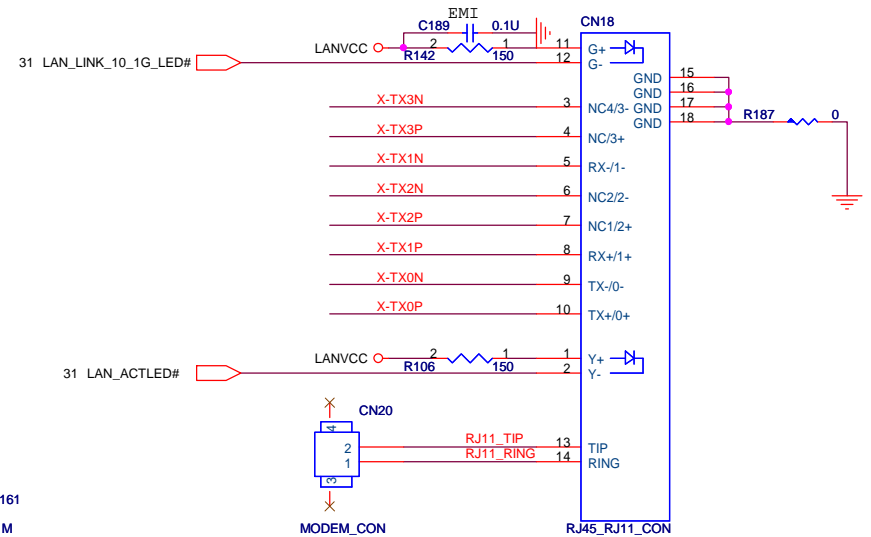
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 BCM5906M(LAN 10/ 100) ==> AJ059060000




10/100M Tr: DBED2LLAN05
10/100/1G Tr: DB0ZH1LAN06

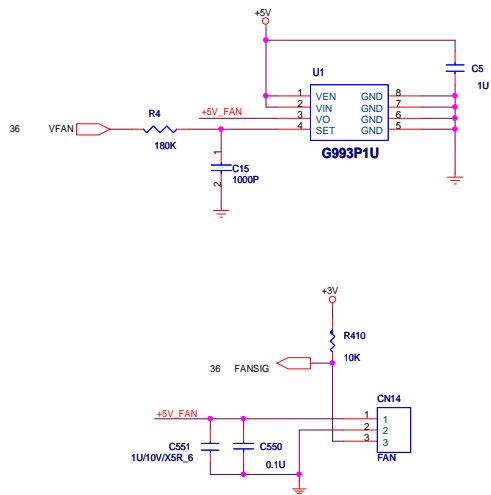


RJ45/RJ11 Connector

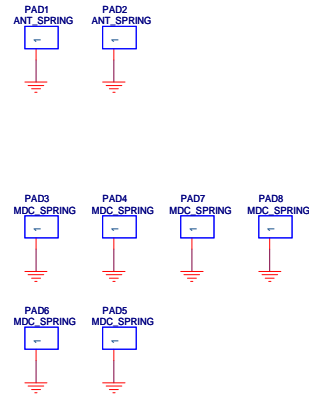


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		Custom	RJ11/RJ45 CONNECTOR	1A
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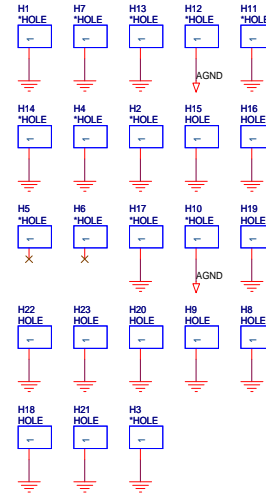
FAN CONTROL



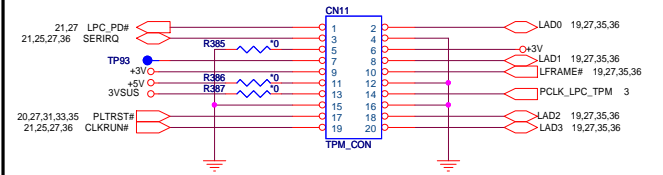
EMI PAD



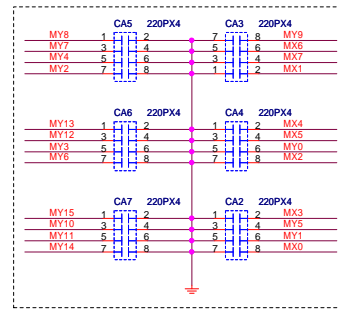
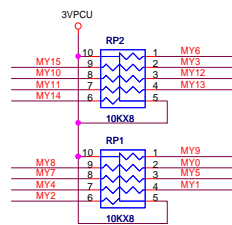
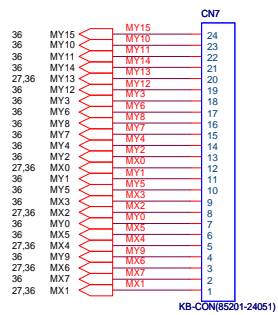
HOLES



Board TO Board TPM MODULE

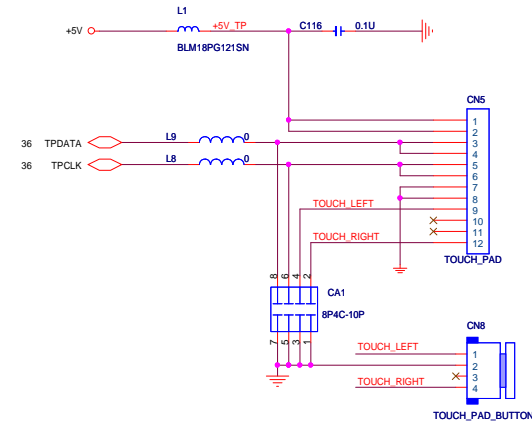



KEYBOARD



For EMI request

TOUCH PAD

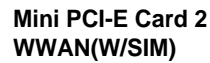




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Quanta Computer Inc.

Size	Document Number	Rev	1A
Custom	FAN, TPM, K/B, T/P		
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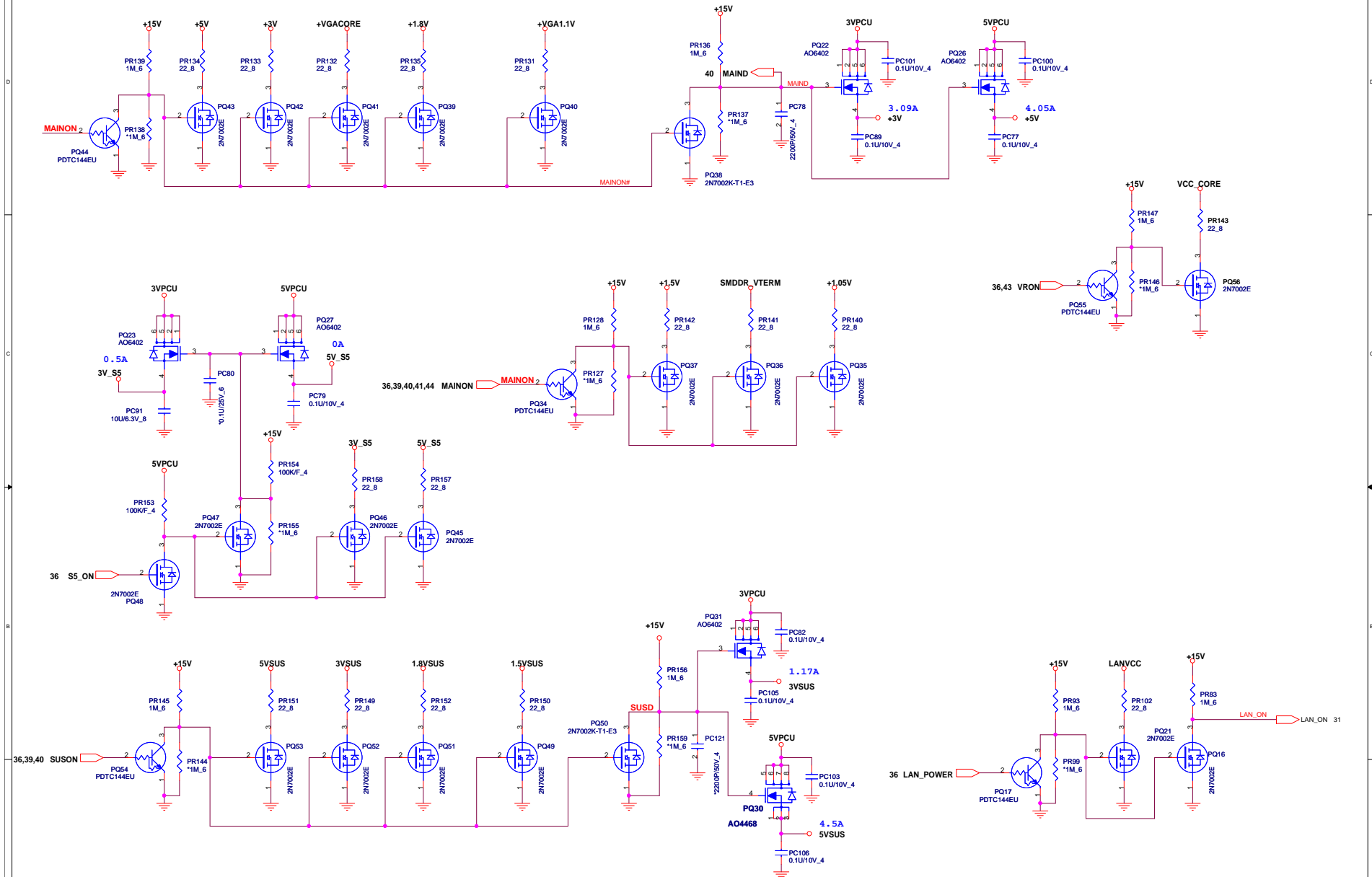
35

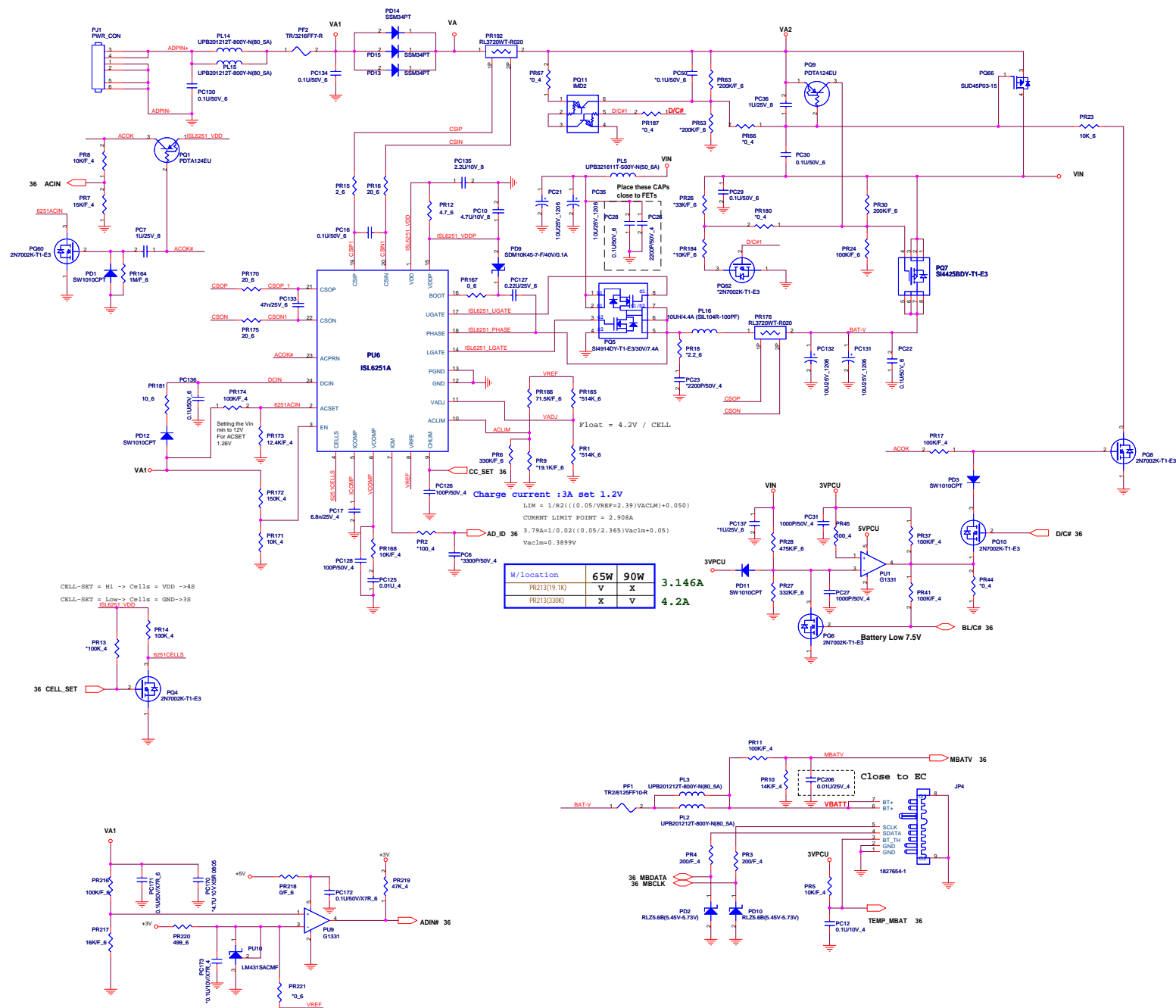


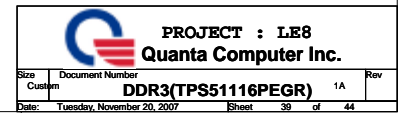
Size Custom	Document Number WLAN & WWAN CON	Rev 1A
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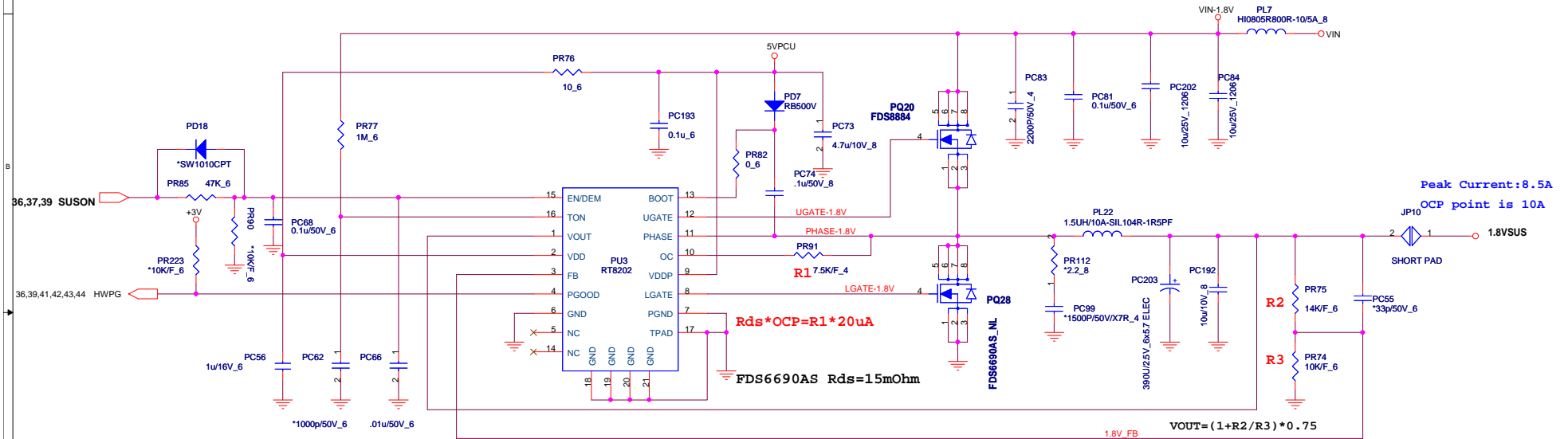


DISCHARGE



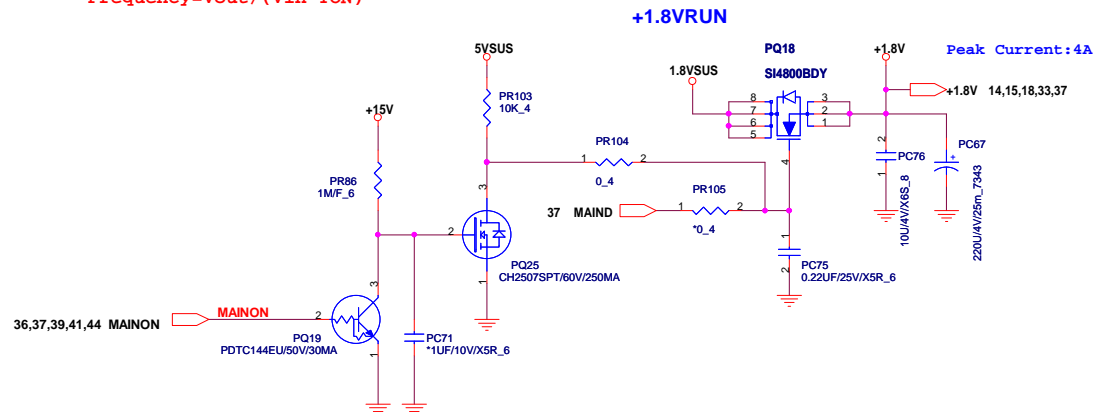




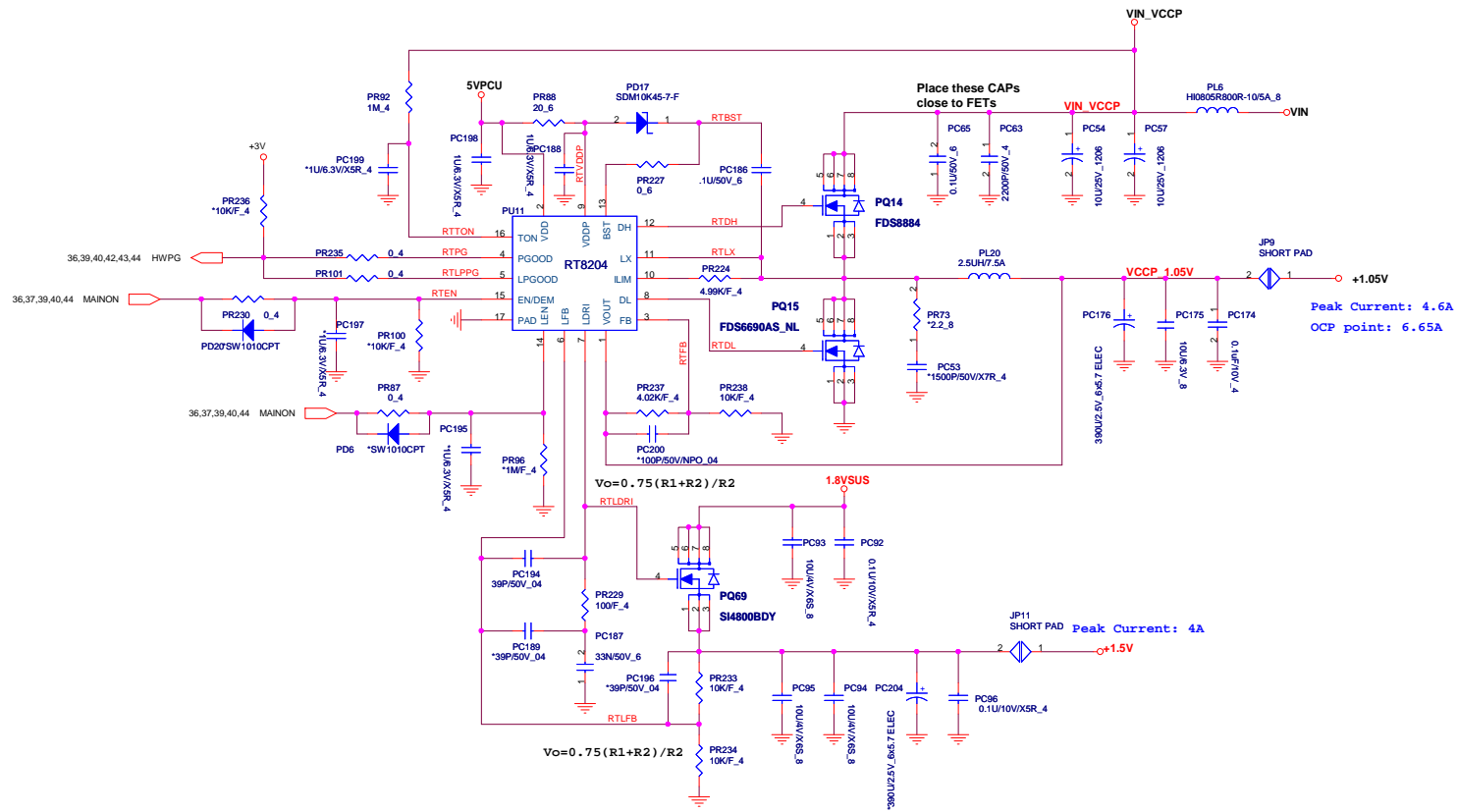


$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

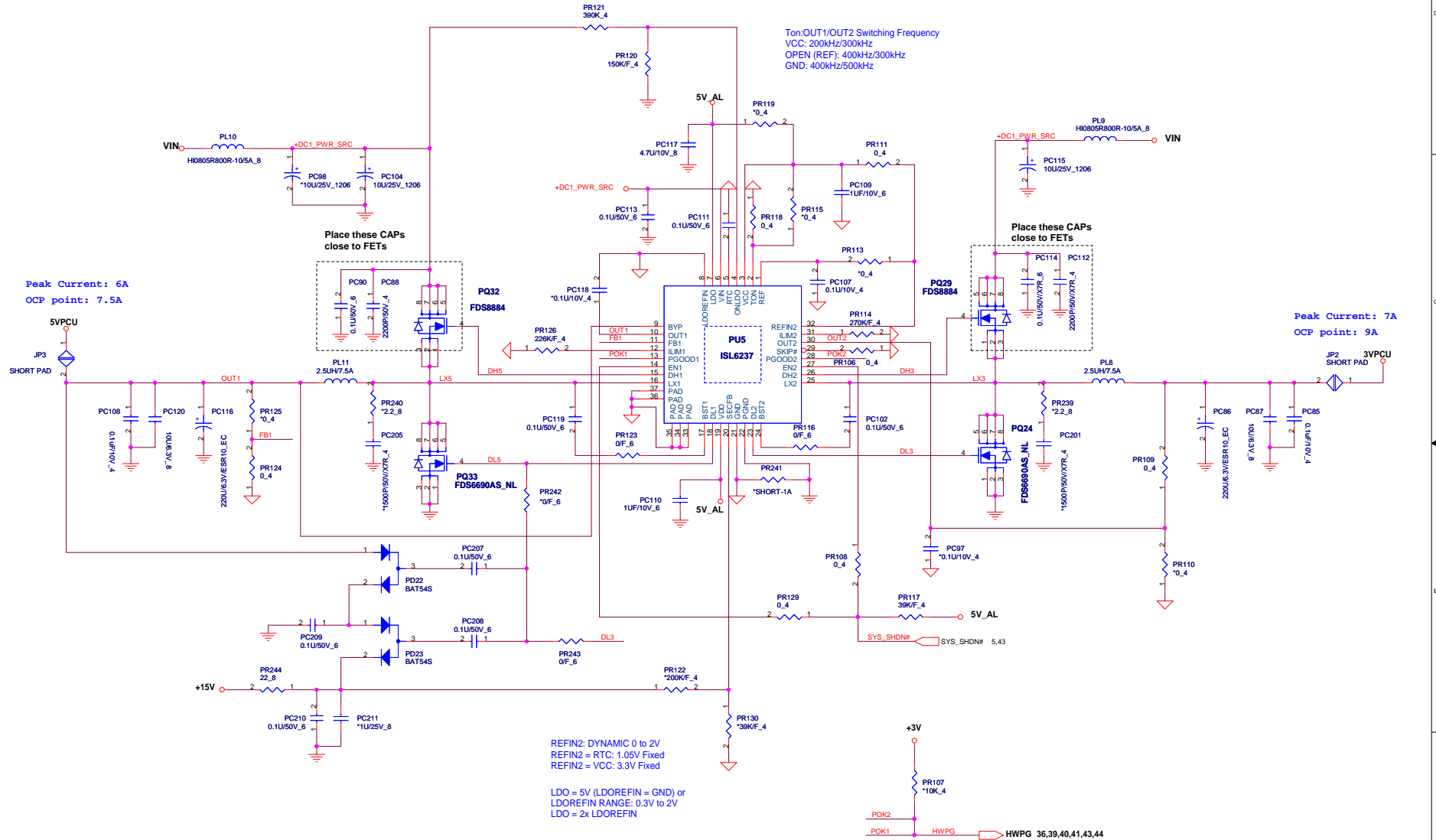
$$Frequency = Vout / (Vin * TON)$$



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		Quanta Computer Inc.	
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DC/DC 3VPCU/5VPCU/+15V



LE8 SYSTEM POWER BLOCK DIAGRAM

